

FIG. 1

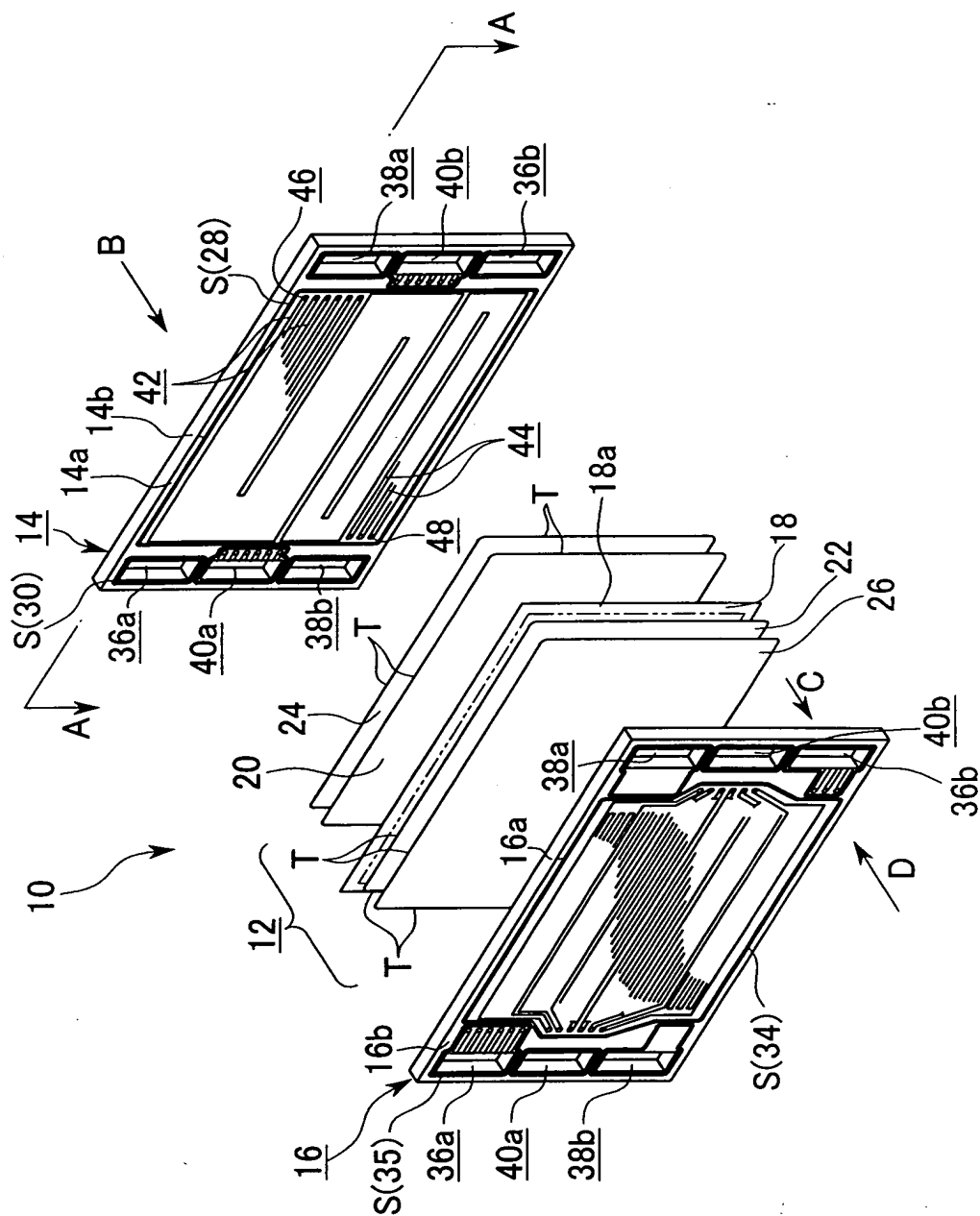


FIG. 2

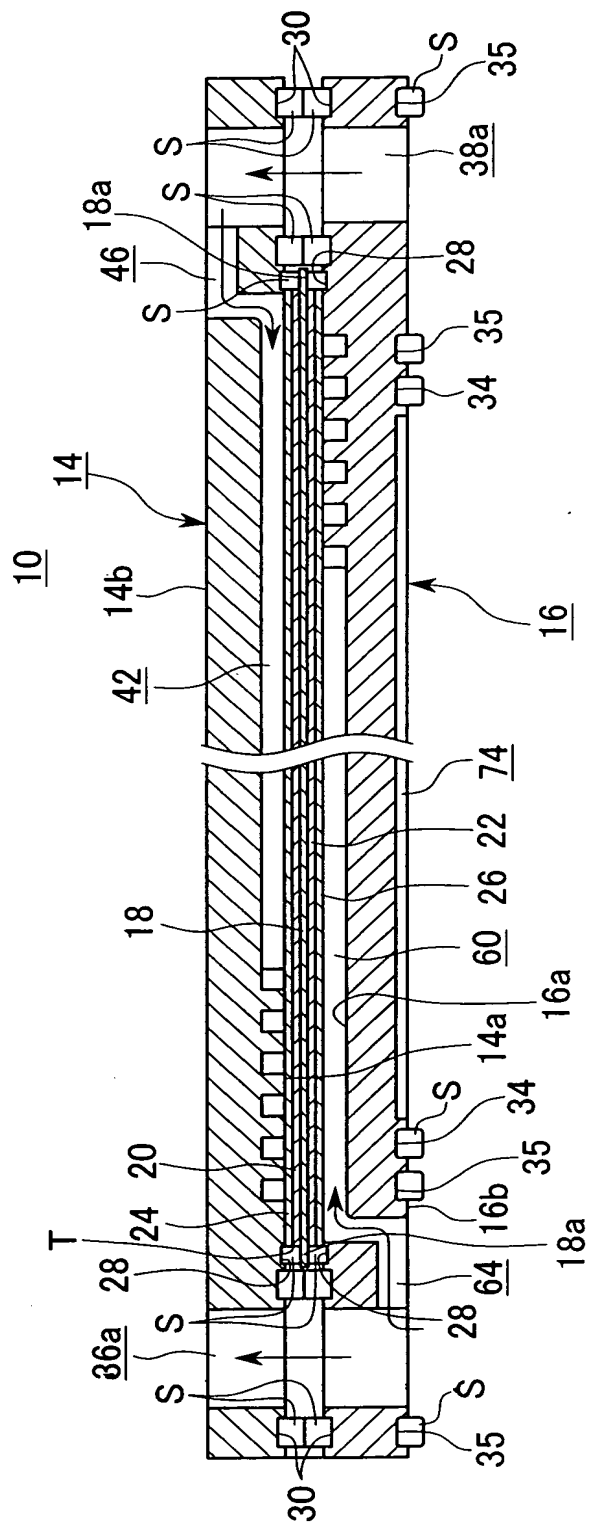


FIG. 3

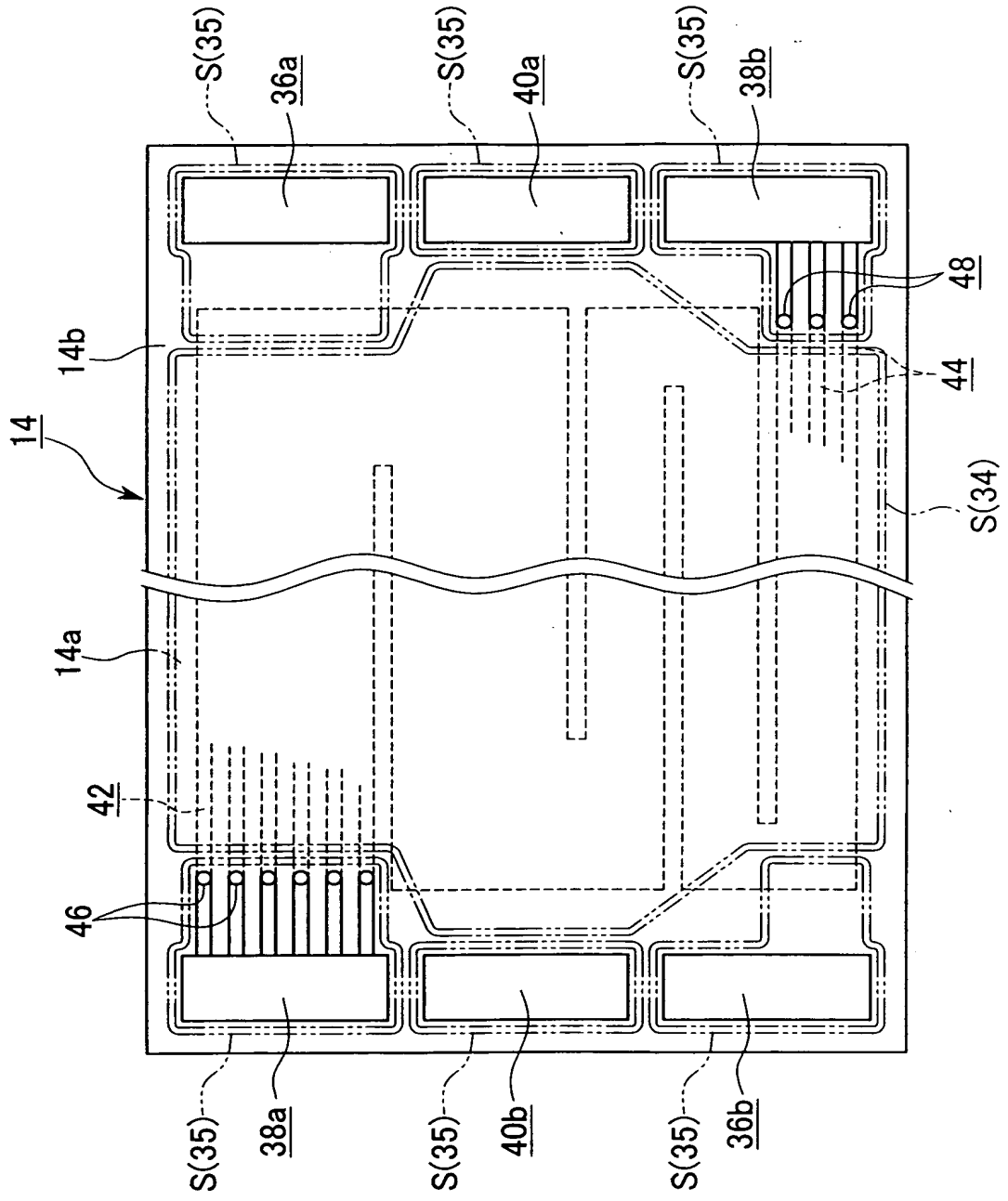
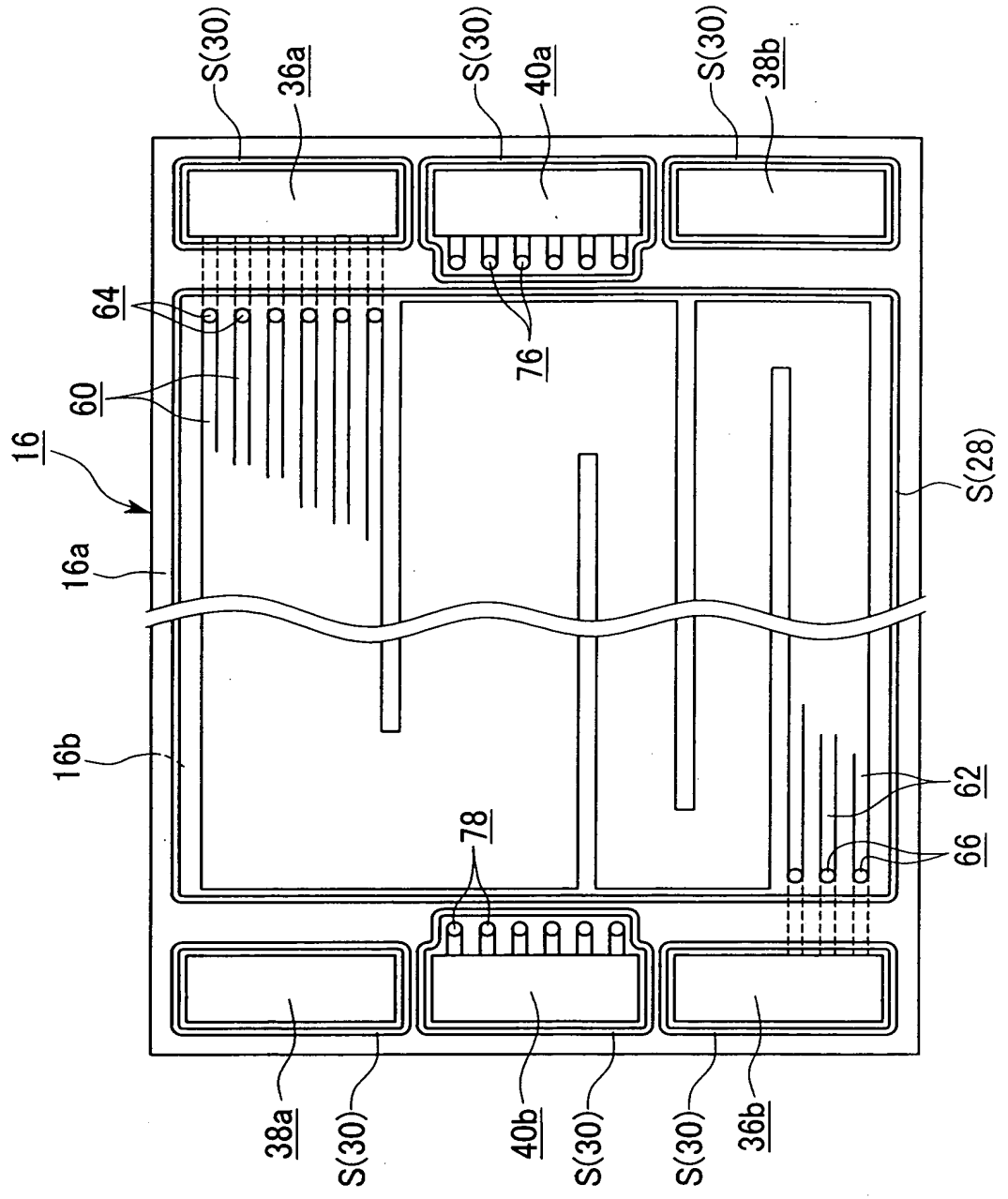


FIG. 4





This diagram shows a cross-sectional view of a semiconductor device. A central channel region, labeled 12, is defined by a series of vertical, hatched segments. This channel is flanked by side gate regions, labeled 14a and 14b, which are shown as rectangular blocks with diagonal hatching. Above the channel, a gate stack, labeled 18, is formed, consisting of a top layer 18a and a bottom layer 18b. The device is embedded in a substrate, labeled 14, which is shown with diagonal hatching. Other labels include 16a and 16b for the side gate regions, 16 for the substrate, 28 for the channel region, and 34 for the top gate region. A dashed line labeled S indicates a surface, and a dashed line labeled T indicates a top surface.

FIG. 7

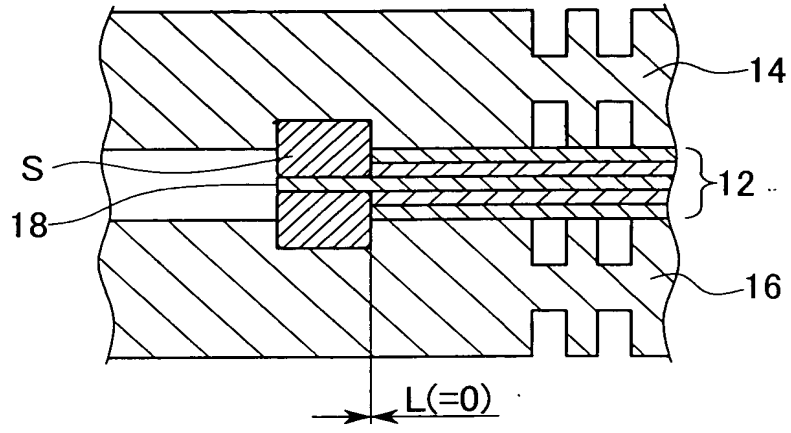


FIG. 8

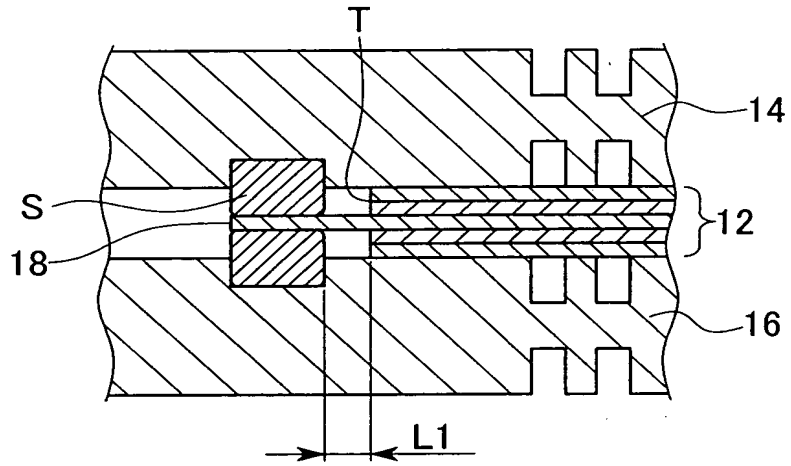
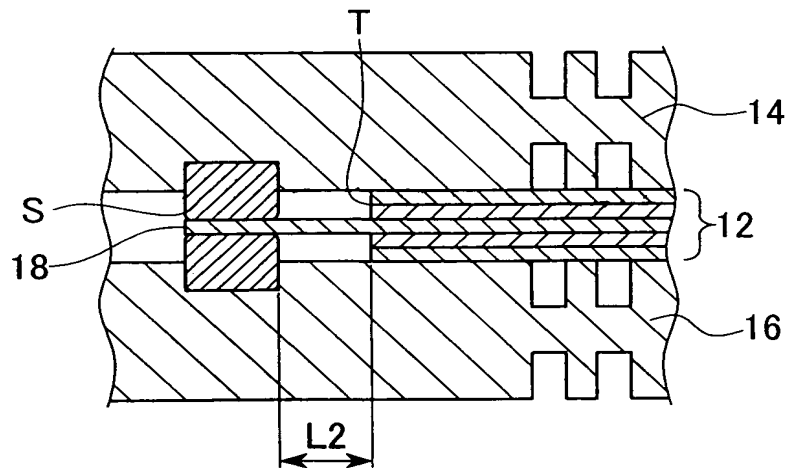


FIG. 9



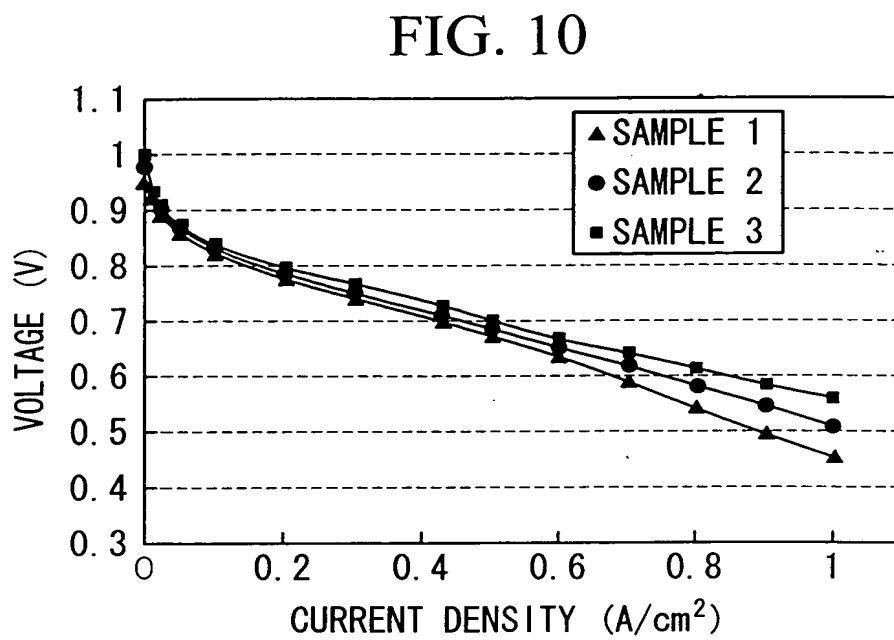


FIG. 11

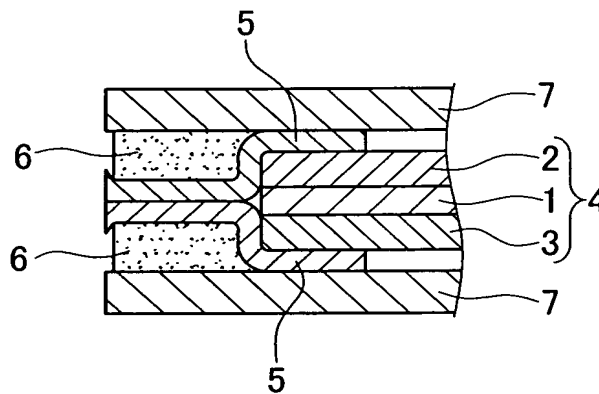


FIG. 12

